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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,688	03/25/2004	Yuichi Gomi	OOCL-154 (6HS-04S0274)	6066

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EXAMINER	
WANG, KENT F	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,688	GOMI ET AL.	
	Examiner	Art Unit	
	KENT WANG	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/09/2009 has been entered.

Response to Amendment

2. The amendments, filed on 01/09/2009, have been entered and made of record. Claims 18 and 19 have been amended, and claim 24 has been added. Claims 18-24 are pending.

Response to Argument

3. Applicant's arguments with respect to independent claim 18 and dependent claims 19-24 have been considered but are moot in view of the newly found prior art references.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 18-19 and 21-22 are rejected under 35 U.S.C. § 102(b) as being unpatented over Nakamura (US 2003/0086005) in view of Ogura (US 2003/0193585), and further in view of Hagihara (US 6,822,211).

Regarding claim 18, Nakamura discloses a solid-state image sensing apparatus comprising:

- an image sensing area (photodiodes 15, Fig 2) in which a plurality of pixels are two-dimensionally arrayed (two-dimensionally arranged in a given pattern) ([0206] and Fig 2);
- a plurality of output channels (four signal charge readout electrode systems V1A,V1B, V3A,V3B, all of which are respectively connected to the vertical transfer path gate signal wirings 18, Fig 2) ([0198]);
- a first driving mode (the full-pixel individual readout mode, the third driving mode) in which pixel signals of pixels in the image sensing area are readout, wherein the read-out pixel signals are output to at least one output channel selected from among the plurality of output channels (V3A or V3B serve as the charge readout electrodes for reading the remaining pixels R, i.e. the pixels R on the other even-numbered horizontal lines, V1A for reading pixels B and V1B for reading pixels G) ([0111] and [0199]);
- a second driving mode (the summation readout mode, the second driving mode) in which pixel signals of odd-numbered columns (odd-even numbered horizontal line) and pixel signals of even-numbered columns (even numbered line) in the image sensing area are read-out ([0111] and [0199]-[0200]); and

- a control circuit (CCD driving circuit 3, Fig 1) which sets driving mode to one of the first driving mode and the second driving mode based on an externally input signal (the CCD driving circuit 3 also functions to receive driving-mode switching signals 101 from the CPU 14 and change the driving mode of the CCD2 based on the driving-mode switching signals 101 thus input into the CCD driving circuit 3) ([0111]), wherein the input signal may be freely set (switching between the two modes can be done very easily) ([0126]),
- wherein the number of output channels to which the pixel signals are output in the first driving mode (the full-pixel individual readout mode) and the number of output channels to which the pixel signals are output in the second driving mode (the summation readout mode) are different ([0198]-[0200], Nakamura).

Nakamura does not specifically teach the pixel signals of odd-numbered columns and pixel signals of even-numbered columns arrayed in the same row in the image sensing area are read-out. However Ogura discloses the pixel signals of odd-numbered columns and pixel signals of even-numbered columns arrayed in the same row in the image sensing area are read-out (the pixel signals read out from odd-numbered columns in a row of pixels 3101 and the pixel signals read from even-numbered columns in the same row are stored in the line memory circuit 3109), wherein the read-out pixel signals are output to a plurality of output channels selected from among the output channels (at each of output terminals 3108 and 3113), and wherein the read-out pixel signals of odd-numbered columns and the read-out pixel signals of even-numbered columns are output to different ones of the selected output channels so as to have different phases (switches 3116 and 3117 connected in parallel are

switched ON/OFF in alternating sequence so as to output pixel signals from the odd-numbered columns of pixels and the even-numbered columns of pixels from the output terminal 3120 via the output buffer circuit 3119) ([0007]-[0014], Ogura).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the signal readout structure as taught by Ogura into Nakamura's image capturing apparatus, as by outputting the dark level signals and the pixel signals are output at the different phases, the output terminals 3108 and 3113 operate at half-cycle with respect to the clock rate at output terminal 3120, the readout speed can be increased relatively easy ([0014], Ogura).

Nakamura and Ogura do not specifically teach the line memories which are arranged between the pixels and the output channels and which temporarily store pixel signals of the pixels selected and read out in the first driving mode or the second driving mode; and a control circuit which is arranged between the pixels and the line memories. However Hagihara discloses the line memories (line memory 10, Fig 1) which are arranged between the pixels (pixel G10, Fig 1) and the output channels (output, Fig 1) and which temporarily store pixel signals of the pixels selected and read out in the first driving mode or the second driving mode (6:18-54, Hagihara); and a control circuit (output switching circuit 9) which is arranged between the pixels (G10) and the line memories (10) (5:41-6:17, Hagihara).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the control and readout circuitry as taught by Hagihara into Nakamura and Ogura's image capturing apparatus, so as to provide a solid-state image-sensing device capable of canceling fixed pattern noise resulting from variations in the output

signals of the solid-state image-sensing device due to the circuit configuration thereof or the like, thus makes it possible to eliminate vertical stripes resulting from the fact that, conventionally, output signal lines are provided one for each column of pixels (2:17-21 and 23:15-23, Hagihara).

Regarding claim 19, Nakamura discloses the control circuit (CCD driving circuit 3, Fig 1) is a transfer switch in which a common control signal is input in every other column (line buffer having the function of a processing unit which is capable of recording image data for one line may be included in the image capturing apparatus) ([0226], Nakamura).

Regarding claim 21, Nakamura discloses the image sensing area is provided with a color filter in Bayer matrix corresponding to the pixels (primary color Bayer arrangement), and in the second driving mode, pixel signals of pixels in the same color phase among color phase codings defined by the color filters are output from the same output channels (the summation readout mode calls for summing up signal charges of the same colors to avoid mixing of colors, the color-mixing summation readout mode calls for mixing and reading out signal charges of pixels of different colors to output signals that are as close to luminance signals as possible, and making use of the output signals for measuring the distance to the subject) ([0162], Nakamura).

Regarding claim 22, the limitations of claim 18 are taught above, Ogura discloses there is a channel which can be used in common (a time division multiplex unit adapted to perform time division multiplexing on signals from the plurality of common readout units so as to output time division multiplexed signals) ([0026], Ogura).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the TDM unit as taught by Ogura into Nakamura's image capturing apparatus, so as the signals from pixels covered with color filters of the same color are multiplexed continuously, thus form an image of superior picture quality which avoids color mixing ([0025]-[0026], Ogura).

6. Claim 20 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakamura (US 2003/0086005) in view of Ogura (US 2003/0193585) and Hagihara (US 6,822,211), and further in view of Yasuyuki Yamazaki (US 5,150,204).

Regarding claim 20, the limitations of claim 18 are taught above, Nakamura and Ogura do not specifically teach the phase shift between the pixel signals of the odd-numbered columns and the pixel signals of the even-numbered columns is 180 degrees. However Yamazaki discloses the phase shift between the pixel signals of the odd-numbered columns and the pixel signals of the even-numbered columns is 180 degrees (pulses having a phase shift of 180 degrees between first and second fields for outputting read-out signals onto a plurality of channels) (1:65-2:8, Yasuyuki Yamazaki).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the readout switching device as taught by Yamazaki into Nakamura and Ogura's image sensor, as to obtain an image of high horizontal resolution without using high precision delay lines as conventional (2:9-18, Yasuyuki Yamazaki).

7. Claim 23 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakamura (US 2003/0086005) in view of Ogura (US 2003/0193585), and further in view of Yoshirou Yamazaki (US 6,496,286).

Regarding claim 23, the limitations of claim 18 are taught above, Nakamura and Ogura do not specifically teach the pixel signals of pixels from m X n pieces in the image sensing area are output wherein m and n are integers. However Yamazaki discloses the pixel signals of pixels from m X n pieces in the image sensing area are output wherein m and n are integers (image reader comprises n pieces of line sensors arranged in parallel in such a way that, with "n" being an integer of 2 or more) (2:31-47, Yoshirou Yamazaki).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the image reader as taught by Yamazaki into Nakamura and Ogura's image sensor, as to provide an image reader capable of increasing a resolution while simply keeping an area of light receiving elements of a sensor to some extent at a low cost (2:25-30, Yoshirou Yamazaki).

8. Claim 24 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakamura (US 2003/0086005) in view of Ogura (US 2003/0193585) and Hagihara (US 6,822,211), and further in view of Yoneda (US 2002/0067416).

Regarding claim 24, the limitations of claim 18 are taught above, Nakamura and Ogura do not specifically teach the line memories are capacitive elements arranged in every column. However Yoneda discloses the line memories (line memory 910, Fig 5) are capacitive elements arranged in every column ([0056], Yoneda).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the line memory as taught by Yoneda into Nakamura, Ogura and Hagihara's image sensor, so as the control signals for sequentially outputting the amplified signals accumulated in each capacitor to the outside are generated in each of the

horizontal shift registers and outputted to the line memory, thus to reduce a lag of time for accumulating photocharges among image pickup areas ([0017], [0067], Yoneda)

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Babuchi (US 7,138,617) discloses a solid-state image pickup device has a differential output configuration for an output stage thereof and an IC in a next stage has a differential amplifier configuration for an input stage thereof;
- Hara et al. (US 7,139,026) discloses an imaging device reads an output level of a pixel circuit constituting a pixel array by supplying current to the pixel circuit; and
- Yoneda et al (US 6,952,228) provides an apparatus capable to reduce a lag of time for accumulating photocharges among image pickup areas.

Inquiries

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kent Wang whose telephone number is 571-270-1703. The examiner can normally be reached on 8:00 A.M. - 5:30 PM (every other Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-270-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://portal.uspto.gov/external/portal/pair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free)? If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan V Ho/
Primary Examiner, Art Unit 2622

KW
19 February 2009